Data Device Corporation

Multi-Protocol PCI Board

Instructions

Version 1.0
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TABLE OF CONTENTS

1.0 Package Contents

One PCI board
Instructions
Software Disks: WindowsNT/95/98 Filght Deck Software
Qukstart.doc
New1582.doc

Flight Deck is menu driven GUI software which controls the PCI board and all the functions of the multi-protocol terminal(s) on the board.

Qukstart.doc is a WORD97 document which demonstrates the use of Flight Deck.

New1582.doc is the manual for the NHi-15382et terminal(s) which are on the PCI board. This is a WORD97 document.

1.1 FEATURES

- Mil-Std-1553 and Multi-protocol PCI Interface Card
- One or Two Independent Dual redundant Multi-protocol BC/RT/MTs on a PCI card
- 1553B Notice 2,STANAG 3838,1760,3818, EFA, etc.
- 64K x 16 Shared RAM for each dual BC/RT/MT
- Programmable BC Gap Times
- BC Frame Auto-Repeat
- RT Data Buffering
- RT Separate Broadcast Data Tables
- Monitor Command Filtering
- Simultaneous RT/Monitor
- Programmable Interrupts
- Low cost solution for 1553B protocol based testing
- On board watchdog timer
- Time tag with programmable resolution
- Programmable real time clock
- Switch selectable interrupt levels
- Low power consumption

1.2 Description

The NHI-15503 is a PCI card which contains one or two completely independent 1553 interfaces. Each interface is an NHi-15382ET multi-protocol MCM . which can operate as an RT, BC, or MT.
Each ET includes two monolithic transceivers, a protocol asic and 64K wordsof shared RAM. Double buffering of the shared RAM enables simultaneous message preparation and 1553 bus transfers

All modes of operation access data tables via pointers residing in RAM which facilitates multiple buffering. This allows buffers to change without moving data and promotes efficient use of RAM space. The data tables have programmable sizes and locations.

The invisibility of memory when the card is not active prevents inadvertent access during power-on-self test of the PC or by any other process.

2.0 INSTALLATION

2.1 Inspection

The card has been thoroughly tested and inspected before shipment.
After removing the card from the packing container, please retain the container as it may be used to store the card when not installed in the computer. The packing container may be utilized in the event that the card has to be returned due to failure or damage.

2.2 System Requirements

SYSTEM REQUIREMENTS
PC with PCI Bus
Windows95/98/NT
Hard disk
Color Monitor

Follow these precautions before installing the card inside your PC. Remove power to the PC before opening the top cover. Make the necessary switch and jumper selections for your application as detailed in this manual and then plug the card into an available slot on the motherboard. The card has been delivered from the factory with the folowwing default settings:

IRQ from the terminals are software disabled
Buses are jumpered for Stub coupling(via jumper blocks),
Hardwire RT address 01 and 02 for terminals 1 and 2 respectively(via jumper blocks).

Follow the installation instructions in file LOAD95.TXT or LOADNT,TXT.

REMOVE POWER TO THE PC WHEN REMOVING OR INSERTING THE CARD INTO THE PC.

2.3 Coupling Transformer Jumpers

The card can be configured for either direct or transformer coupling via jumpers JP13-JP20.

For terminal 1: jumpers JP13 and JP14 are for Bus A,
jumpers JP15 and JP16 are for Bus B

For terminal 2: jumpers JP17 and JP18 are for Bus A,
jumpers JP19 and JP20 are for Bus B

The jumper configuration for the coupling transformer for each terminal is shown below:

Jumper	Transformer Coupling	Direct Coupling
JP13		
JP14		
JP15		
JP16		
JP17		
JP18		
JP19		
JP20		

Note:
In the above illustration, position the PCI card with the component side up and the Bus connectors are on your left.

Both Bus A and Bus B of each terminal should be configured the same way to avoid any potential bus mismatch.

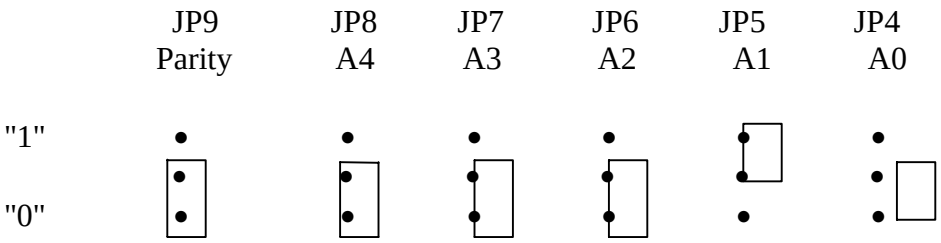
2.4 Hardwired RT Address Jumpers

Each of the Terminals can be given a unique Remote Terminal(RT) hardwire address via jumper selection.

The configuration for terminal 1 with an RT address of 1 and odd parity is shown below:

	JP3 Parity	JP2 A4	JP1 A3	JP12 A2	JP11 A1	JP10 A0
"1"						
"0"						

The configuration for terminal 2 with an RT address of 2 and odd parity is shown below:



Note:
In the above illustration, position the PCI card with the component side up and the Bus connectors are on your left. "1" is at the top of the jumper block.

3.0 ADDRESS MAP

The following memory map information is not generally required by a user unless custom software is being developed for the NHi PCI card.. The NHi Filght Deck Windows software handles all memory allocation and accesses.

Each terminal on the 15503 card appears to the host as 64K words of contiguous memory. The address map for each terminal is shown below.

ADDRESS (in words)

0-29	Internal Control and Status registers
30	External RT address / Command outpin pins
31	Not Used
32-35	Not Used
64- 65535	Shared RAM (accessed on the Host I/O bus)

The following address map table defines all addresses relevant to the user. The addresses are offsets from the base address as selected by the user.

ADDRESS	CONTENTS/OPERATION	R/W
Base + 0	Control Register	R/W
Base + 1	Pointer Table Address Register	R/W
Base + 2	Basic Status Register	R/W
Base + 3	IMR (lower byte)	R/W
Base + 3	IVR (upper byte)	R
Base + 3	IRR (upper byte)	W
Base + 4	IVR (lower byte)	R/W
Base + 4	AVR (upper byte)	R
Base + 4	Configuration Register 2 (upper byte, BC/MT only)	W
Base + 5	RTC_ High	R
Base + 6	RTC_ Low	R
Base + 7	RTC Control Register	R/W
Base + 8	FIFO Read	R
Base + 8	FIFO Reset (both bytes)	W
Base + 9	Configuration Register 1	R/W
Base + 10	Reserved	
Base + 11	Last Command Register	R
Base + 12	Last Status Register	R
Base + 13	Frame “A” (Msg List Addr)/ Block “A” Start Address	R/W
Base + 14	Frame “A” Length (Msg List Len)/Block “A” End Addr	R/W
Base + 15	Reset RT (both bytes)	W
Base + 16	Frame “B” (Msg List Addr)/ Block “B” Start Address	R/W
Base + 17	Frame “B” Length/ Block “B” End	R/W
Base + 18	Encoder Status Register	R
Base + 19	Condition Register	R
Base + 20	BC Frame Gap/ Word Monitor End of Frame Options	R/W
Base + 21	Configuration Register 3	R/W
Base + 22	Message Monitor Address Filter 1 (0-15)	R/W
Base + 23	Encoder Data Register *	R/W
Base + 24	Encoder Data TX Request (both bytes) *	W
Base + 25	Encoder CMD TX Request (both bytes) *	W
Base + 26	Message Monitor Address Filter 2 (16-31)	R/W
Base + 27	Word Monitor Last Address Block “A”	R
Base + 28	Word Monitor Last Address Block “B”	R
Base + 29	Reserved	
Base + 30	External RT Address Buffer (lower byte)	R
Base + 30	Command Output Pins	W
Base + 31	I/O Tag Register	R/W

* In order to write to addresses 23, 24, and 25, the ET must be in loopback in the RT mode (see Control Register in the Enhanced Terminal Products User’s Manual for details).

4.0 HARDWARE DESCRIPTION

4.1 Clock

A 20 Mhz oscillator (U4) is used to provide the required clocks for the NHi-15503 PCI Card.

4.2 PCI To Local Bus Bridge

A PLX9050 chip is used as the PCI to local bus bridge. It interfaces with the two NHi-ET's and and Altera EPM7064 pld. The EPM7064 connects the local bus and control signals to each NHi-ET.

4.3 NHi-15382ET Terminals

The PCI card contains two NHi-15382ET terminals which function as a BC, MT, RT or an MT/RT. See the NHi Enhanced Terminals Manual for a full description.

5.0 On-Line Help

On-Line help is available for all menu items and dialog boxes. Use the left mouse button
to drag the Question Mark(?) to the item requiring help; then release the button over that item. The help dialog will appesr in the upper left screen area.

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